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Term: L6 and (circuit with (task adj scheduler))

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L10	L6 and (hardware$ with (task adj scheduler))	2	L10
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L7	L6 and (circuit$ with task$ with schedul$ with priority)	2	L7
L6	(computer$).ab.	56215	L6
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L4	L2 and (circuit$ with priority with task$ and management)	2	L4
L3	L2 and (priority with task$ and management)	299	L3
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Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: US 4642756 A

L9: Entry 1 of 1 File: USPT Feb 10, 1987

Alt -> task scheduler

DOCUMENT-IDENTIFIER: US 4642756 A
TITLE: Method and apparatus for scheduling the execution of multiple processing tasks in a computer system

Abstract Text (1):
A task schedular for scheduling the execution of a plurality of tasks within a computer system. The task scheduler utilizes a combination of externally assigned priorities and internally calculated priorities to optimize the responsiveness of the computer to external interactions.

Detailed Description Text (3):
As shown in FIG. 3, the task scheduler of the present invention comprises logic circuit 7', RAM memory 8', ROM memory 9', parameters registers 12', RUNTIME timer 10', INTTIME timer 11' and counters 14'. Logic circuit 7' performs all of the logical computations required to establish the order in which the various tasks stored in RAM 1' and ROM 2' (FIG. 2) as user programs are to be executed by CPU 5' based on task priorities. Logic circuit 7' then instructs CPU 5' as to which tasks should be executed and for how long. The functions performed by logic circuit 7' can be handled by a microprocessor selected from among those known in the art. CPU 5' can also perform these functions but the time spent by the CPU in doing so diminishes the CPU time available for performing tasks for system users. RAM 8' and ROM 9' store the instructions and data required by logic circuit 7' to carry out its functions. Parameter registers 12' store task scheduling parameters used by the task scheduler, RUNTIME timers 10' and INTTIMER timer 11' are elapse timers used by the task scheduler and counters 14' are event counters also used by the task scheduler.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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Term	Documents
CIRCUIT.USPT.	799106
CIRCUITS.USPT.	423753
TASK.USPT.	106897
TASKS.USPT.	54793
SCHEDULER.USPT.	4536
SCHEDULERS.USPT.	591
(((TASK ADJ SCHEDULER) WITH CIRCUIT) AND 6).USPT.	1
(L6 AND (CIRCUIT WITH (TASK ADJ SCHEDULER))).USPT.	1

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Search Results - Record(s) 1 through 2 of 2 returned.

☐ 1. Document ID: US 4628158 A

L7: Entry 1 of 2 File: USPT Dec 9, 1986

Circuit → sched, task, priority

DOCUMENT-IDENTIFIER: US 4628158 A
TITLE: Stored program controller

Abstract Text (1):
A mechanized system distributing the access, test and communication functions to the point of testing, typically the centralized switching facility serving the telephone loops and equipment to be tested. Computer (200) stores information about each subscriber loop in the geographical area served by a system. Front-end computers (220,221) interact with computer (200) to retrieve pertinent data regarding loops to be tested. Each switching facility in an area includes a loop testing system (e.g., 160) that implements the required functions. The communication functions residing in front-end computers (220,221) and loop testing systems (160,161) are coupled via a data communication network (140) in a manner that allows any front-end computer to communicate with any loop testing system. Users of the system control access and test from consoles having the capability of establishing independent communication paths over the national dial network for interactive tests on loops accessed through standard test trunks. Microprocessor-based circuitry is utilized for numerous system tasks such as signal generation, digital signal processing and controlling sensitive analog measurements. Signal generation includes digital generation of analog waveforms. Signal processing techniques incorporate various digital filters to analyze sample sequences derived from, for example, dial pulses and coin telephone signals. Sensitive analog measurements of loop characteristics are effected with a magnetic current detector that operates over broad current and frequency ranges. Frequency dependent measurements are converted to DC using synchronous demodulation techniques to enhance resolution.

CLAIMS:

1. In a data communications or telephone system, a controller for processing a series of request messages received over an input bus and for distributing corresponding command messages of predetermined types derived from each of said request messages over output busses connected to said controller, said controller comprising

microprocessor means (e.g., 2045) having an accessible memory, interrupt processing circuitry (510) including an interrupt processing routine to signal the completion of events and a multitasking operating system including means for scheduling, according to a predetermined priority, corresponding tasks to be initiated as a result of said completion of events,

input means (e.g., 2070), connected to said input bus and serviced at interrupt level by said microprocessor means, for assembling said command messages by interpreting each of said request messages, for storing said command messages in allocated buffers in said memory and for signaling message-complete events, and

output means (e.g, 2045), connected to said output busses and serviced at interrupt level by said microprocessor means, said output means including a task processor associated with each of said command message types for accessing an associated one of said buffers as directed by said microprocessor means, for extracting said

corresponding command message, and for formatting and transmitting each said corresponding command message over one of said output busses.

☐ 2. Document ID: US 4539652 A

L7: Entry 2 of 2 File: USPT Sep 3, 1985

DOCUMENT-IDENTIFIER: US 4539652 A
TITLE: Networks for data communication

Abstract Text (1):
A mechanized system distributing the access, test and communication functions to the point of testing, typically the centralized switching facility serving the telephone loops and equipment to be tested. Computer (200) stores information about each subscriber loop in the geographical area served by a system. Front-end computers (220,221) interact with computer (200) to retrieve pertinent data regarding loops to be tested. Each switching facility in an area includes a loop testing system (e.g., 160) that implements the required functions. The communication functions residing in front-end computers (220,221) and loop testing systems (160,161) are coupled via a data communication network (140) in a manner that allows any front-end computer to communicate with any loop testing system. Users of the system control access and test from consoles having the capability of establishing independent communication paths over the national dial network for interactive tests on loops accessed through standard test trunks. Microprocessor-based circuitry is utilized for numerous system tasks such as signal generation, digital signal processing and controlling sensitive analog measurements. Signal generation includes digital generation of analog waveforms. Signal processing techniques incorporate various digital filters to analyze sample sequences derived from, for example, dial pulses and coin telephone signals. Sensitive analog measurements of loop characteristics are effected with a magnetic current detector that operates over broad current and frequency range. Frequency dependent measurements are converted to DC using synchronous demodulation techniques to enhance resolution.

CLAIMS:

1. A bus connection system (141,1421-1432,145,14001-14096) for connecting a plurality (M) of input busses (14101-14103) having a message format to a plurality (N) of output busses (93001-93768) having a data format, said system comprising

a plurality (I) of first program control means (1421-1432), each identified by a logical identifier (L.sub.2 =0, 1, . . . , I-10) and associated with an interface bus having a communication format (e.g., GPIB),

a plurality (J) of second program control means (14001-14096) arranged into a preselected number (I) of sets, wherein in each of said sets each of said second control means is identified by a logical identifier (L.sub.3 =0, 1, . . . , N/J-1) and is coupled to said interface bus of a corresponding first control means,

said first control means and said second control means each having processor means (550,570) with accessible memory (520,530,540), interrupt circuitry (510) including an interrupt processing routine to signal the completion of events and a multitasking operating system (OS) including a task scheduler (SCHEDULER) for scheduling, according to a predetermined priority, corresponding task issuing as a result of said event completions,

said first control means including first input bus control means (710,720), connected to one of said input busses and serviced by its associated identified task scheduler in response to its associated interrupt processing routine, for receiving and storing said messages (INFORMATION fields) in an area of its associated memory assigned to said one of said input busses whenever said messages (`down.sub.-- route`) contain said identifier assigned to said each of said first control means, for augmenting said stored messages with routing parameters (`up.sub.-- route`) identifying which of said input busses transmitted said received messages and for signaling message-complete events,

said first control means including first interface bus control means (620'), connected to said interface bus and serviced by its associated task scheduler in response to its associated interrupt processing routine, for storing communications (INFORMATION fields) received over said interface bus in a memory location determined by parameters (`up.sub.-- route`) in said communications, for transmitting each of said augmented messages over said interface bus and for signaling message-complete events,

said first input bus control means including means (710,720) for transmitting communications from each said memory location over the associated one of said input busses,

said second control means including second input means (710',720'), serviced by its associated task scheduler in response to its associated interrupt processing routine for receiving and storing communications (INFORMATION fields) arriving over said interface bus in an area of its associated memory assigned to said interface bus whenever said communications (`down.sub.-- route`) contain said identifier assigned to said each of said second control means and for signaling message-complete events,

said second control means including output bus control means (761-768,751-753), connected to a preselected numbeer (N/J) of said output busses and serviced by its associated task scheduler in response to its associated interrupt processing routine, for storing data (INFORMATION fields) received over each of said preselected output busses in a memory location determined by parameters (`up.sub.-- route`) in said data, for transmitting said communications from said assigned memory over the corresponding one of said preselected output busses identified by routing parameters (`down.sub.-- route`) in each of said communications and for signaling message-complete events,

said second interface bus control means including means (710',720') for transmitting data from each said corresponding location in memory over said interface bus.

L1: Entry 142075 of 142075 File: USPT Aug 31, 1971

DOCUMENT-IDENTIFIER: US 3602702 A
TITLE: ELECTRONICALLY GENERATED PERSPECTIVE IMAGES

Detailed Description Text (168):
Thus, one embodiment for carrying out the novel method and system for the present invention has been disclosed. In addition, suitable circuits to carry out the various functions have been either disclosed in detail or known circuits have been referenced. Of course, other circuits for performing the same functions may be utilized. One such arrangement might include the microprocessor units disclosed in the second embodiment of the Romney et al. application cited above. Other suitable circuits will be apparent to those skilled in the art.

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Search Results - Record(s) 100 through 108 of 108 returned.

☐ 100. Document ID: US 4837842 A

L2: Entry 100 of 108 File: USPT Jun 6, 1989

DOCUMENT-IDENTIFIER: US 4837842 A
TITLE: Character and pattern recognition machine and method

Detailed Description Text (50):
FIG. 6 shows details of a recognition scoring device 12. This is an expansion of FIG. 3, which discusses the functions from a block diagram point of view. The preferred embodiment of the Recognition Scoring Device 12 is a serial computer of the classical Von Neuman type. It includes a Best Feature Storage device 60, a Central Processing Unit 61, an Equation and Control Storage Device 62, and an Output Storage device 63.

Detailed Description Text (51):
When the Artificial Fovea of FIGS. 1, 2, and 5 has finished its work it outputs the Best Features found in the pattern to the CPU 61, which in turn stores them in the Random Access Memory (RAM) called Best Feature Storage 60. CPU 61 then procedes to evaluate the Equations which are stored in Read-Only-Memory (ROM) 62. This all is done under the control of the Program, which also resides in ROM 62. The sorting of the equation scores and the acceptibility testing is also done under control of the program in CPU 61. The name of the Accepted Class, plus instructions about what to do if the character is rejected, are all stored in a section of RAM called Output Storage 63. The separation of RAM shown in FIG. 6 is made only for illustrative purposes, and many other assignments may be used. There is no specific reason, for example, why Equation and Control Storage 62 cannot also be RAM"; since the information stored in that memory does, in fact, change less often than the information stored in memories 60 and 63, the use of ROM" is indicated on grounds of higher performance at less cost. Although the use of special purpose hardware designed specifically to perform the recognition scoring function is perfectly possible, the preferred embodiment is a general purpose computer because of the economies possible. Its high degree of flexibility is also valuable. The only drawback is using a general purpose computer here is its speed, which is slow compared to dedicated hardware. If speed becomes a problem, it is quite easy to add more microprocessor computers in parallel to perform the Recognition Scoring function.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

☐ 101. Document ID: US 4814973 A

L2: Entry 101 of 108 File: USPT Mar 21, 1989

DOCUMENT-IDENTIFIER: US 4814973 A
TITLE: Parallel processor

Other Reference Publication (7):
J. Bockus, "Can Programming be Liberated from the Von Neuman Style ?", ACM Turing Award Lecture 1977.

Other Reference Publication (9):
M. Pease, "The Indirect Binary n-Cube Microprocessor Array", IEEE Transactions Computers, vol. C-26, No. 5, 5/1977.

Other Reference Publication (11):
J. Hayes, "A Microprocessor-Based Hypercube Super-Computer", 1986 IEEE, pp. 6-17.

☐ 102. Document ID: US 4644461 A

L2: Entry 102 of 108 File: USPT Feb 17, 1987

DOCUMENT-IDENTIFIER: US 4644461 A
TITLE: Dynamic activity-creating data-driven computer architecture

Brief Summary Text (3):
Basic digital computing operates in the cycles shown on FIG. 1. In what is referred to as a Von Neuman computer a sequence of instructions are alternately fetched from their location in memory into an execution register and executed. The computational sequences begin by providing the computer with a first instruction address for execution. Thereafter, the address of the next instruction is automatically calculated byy the hardware as a result of the previous execution.

Brief Summary Text (4):
A simple Von Neuman system is shown in FIG. 2. The arithmetic and control unit 10 sequentially fetches and executes a series of instructions located in instructional memory 12. Typically, the instructions from memory 12 cause the arithmetic and control unit 10 to operate on data read in through input lines and/or maintained in data memory 14. The results of the calculations can be output to be seen by an operator on a device such as typewriter 16.

Brief Summary Text (5):
Certain computational projects of large magnitude have traditionally imposed severe time constraints on computational ability. Things such as major conversion problems and military command and control systems requiring repetitive, rapid, and immediate results fall into this category. To solve such problems, the Von Neuman type computer has been made bigger and bigger and faster and faster. Recently, much thought has been given to deviating from this approach and having the data drive the problem rather than the problem drive the data. Much of the impetus for research in this area has been as a result of recent developments in hardware wherein microprocessors and "smart" chips have been made available in smaller and smaller sizes and at lower and lower costs. Such an approach is shown in its simplest form in FIG. 3. In such a system, the driving data elements are referred to as tokens. The tokens cause the "firing" of an activity which generates results depending upon the value of the tokens. Assume that an activity is implemented by a separate chip, and that chip 18 has two inputs 20 and 22 and an output 24. Assume further that chip 18 in the presence of both inputs 20, 22 will produce their sum at the output 24. The activity of chip 18 is simply that of the summing of the inputs.

Brief Summary Text (6):
Such a series of activities can be hard-implemented as "activity chips" or can be treated as logical entities emulated by more general devices, such as microprocessors 26 which are shown interconnected in FIG. 4 in what is referred to as a Petri net. Each of the activities 26 performs a function (indicated as f.sub.1

-f.sub.5 respectively) on the input(s). Such Petri nets are pre-established and do not change during the course of a computation. Each of the activities 26 is independent and, therefore, the sequence of computations is a function of the arrival of the tokens. When tokens A and B are present and available for function f.sub.1, its output is available as a input to functions f.sub.2 and f.sub.4. Token C in the presence of the output of function f.sub.1 will cause function f.sub.2 to be calculated providing the second input for function f.sub.4 which, in turn, provides one of the two inputs required for function f.sub.5. The presence of tokens D and E cause the output of function of f.sub.3 to be made available as the second input for function f.sub.5.

Brief Summary Text (7):
Turning now to FIG. 5, a simplified drawing of a computer system of the Von Neuman type as used in real-time on-line systems is shown. The main memory 30 as accessed by the arithmetic and control unit (not shown) contains resident system programs 32, resident sub-routines 34 (usually re-entrant i.e., more than one program can be using them at a time), and a large section of available memory 36 wherein programs can be loaded for temporary execution. The majority of the programs and data are maintained on a mass storage device 38. When, as a result of an appropriate stimulus such as an interrupt, data arrival, or the like, the resident system program 32 requires the execution of a program on the mass storage device 38, that program is transferred from the mass storage device 38 into an unoccupied portion of available execution memory 36 as symbolized by the dotted area 40. When the program has been transferred into area 40, control is transferred to the first instruction and execution proceeds normally. During the execution procedure, the program within dotted area 40 can employ one or more of the sub-routines 34. When the program has completed its operation, dotted area 40 is merely returned to available status. That is, programs are not transferred back to mass storage 38. In the preferred mode of operation of such systems, the programs on mass storage device 38 are maintained in "dump" format and coded according to "run anywhere" techniques. Thus, a simple block transfer from mass storage 38 into execution memory 36 can be accomplished and the program will run wherever loaded. Moreover, the program can be located and operated simultaneously in more than one available area within memory 36.

Brief Summary Text (11):
In a single computer of the Von Neuman type, the problem cannot occur because any word in memory will always be completely accessed. That is, a word in memory will always be written into completely or read completely. In an interrupt-operated system having different priority levels, recognition of the potential problem being discussed herein is recognized by the technique of "re-entrant" coding which must be employed whenever common data can be accessed by multiple programming levels. Still in all, even in that case, reading and writing are on a complete word basis.

Brief Summary Text (14):
It is the object of the present invention to provide a data driven computer architecture having the benefits of data driven initiation with the flexibility of more traditional Von Neuman computers.

Drawing Description Text (2):
FIG. 1 is a block diagram of a prior art computing cycle of the Von Neuman type wherein the operating instructions are alternately fetched and executed.

Drawing Description Text (3):
FIG. 2 is a block diagram of a prior art computer system of the Von Neuman type.

Drawing Description Text (6):
FIG. 5 is a simplified drawing of a prior art computer system of the Von Neuman type as used in real-time on-line systems.

Detailed Description Text (37):
The processors 70 themselves, then, are independent computers which interface to the overall system as shown. It should be recognized that a conventional computer, whether it be microprocessor or an enormous mainframe containing dozens of central processors, can be considered a single "processor" 70 in this machine. Exactly what the processor 70 looks like is not directly relevant to the present invention, which

is more concerned with the interconnection of functionally-specified processors and the overall scheme used to co-ordinate them to work on a single specific user program. The processors 70 must be capable only of carrying out activities 78. Exactly how they do this is actually a "soft" specification, as almost any conventional computer can be programmed to perform that function, qualifying it for a position in this invention. More likely, however, a new design will emerge for these processors 70 for each new implementation of the present invention, disguising this "soft" specification as a "hardware" one. This is rhetorical, as the equivalence of one conventional computer to another is well understood in the art. The present invention encompasses any device which is capable of causing the effective functional " firing" of activities 78. It is sufficient here to note that a conventional computer can do this job.

Other Reference Publication (1):
H. Nichols et al., "DISCUS--A Distributed Control Microprocessor System", Royal Signals & Radar Estab., Procurement Executive, Ministry of Defence, North Site, Malvern, Worcs., UK, 1979.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw Desc | Image

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☐ 103. Document ID: US 4626825 A

L2: Entry 103 of 108 File: USPT Dec 2, 1986

DOCUMENT-IDENTIFIER: US 4626825 A
TITLE: Logarithmic conversion apparatus

Detailed Description Text (2):
Referring to FIG. 1, there is shown a block diagram of a digital signal processor 10. The digital signal processor 10 has a address bus 12 and a data bus 14, each sixteen bits wide, connected thereto for communication with other digital apparatuses, such as memory and other microprocessors.

Detailed Description Text (6):
As is common in all von Neuman machines, program and data are stored in memories (not shown), outside the processor 10, which are accessed by the address bus 12 and the data bus 14. When a program instruction is fetched, it is supplied on the data bus 14 and is loaded into the program cache memory 26. When data is fetched, it is supplied on the data bus 14 and is supplied to the data register file 20. The address for the memory location which contains either program or data is supplied on the address bus 12.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw Desc | Image

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☐ 104. Document ID: US 4583164 A

L2: Entry 104 of 108 File: USPT Apr 15, 1986

DOCUMENT-IDENTIFIER: US 4583164 A
TITLE: Syntactically self-structuring cellular computer

Brief Summary Text (71):
One promising approach is that proposed recently by Mago in U.S. Pat. No. 4,251,861 and in "A network of microprocessors to execute reduction languages," two parts,

International Journal of Computer and Information Sciences 8, 5 (October 1979) and 8, 6 (December 1979). His computer architecture is designed specifically to execute an applicative programming language such as the Formal Functional Programming (FFP) languages introduced by Backus in "Can programming be liberated from the von Neumann style? A functional style and its algebra of programs," Communications of the ACM 21, 8 (August 1978), 613-641. These documents by Mago and by Backus are incorporated here by reference. An FFP language is defined by a small set of syntactic and semantic rules, with useful mathematical properties for reasoning about programs written in the language. FFPs are applicative (expression-oriented) rather than imperative (statement-oriented). There are no variables and no statements. Powerful operators can be built from simpler operators in a uniform style not possible in conventional programming languages. Most importantly, parallelism is easily and naturally expressed.

Brief Summary Text (97):
The Mago machine is essentially a binary tree of microprocessors, with additional connections between adjacent leaf cells. The leaf cells are called L cells (for Leaf, or Linear), and collectively are known as the L array. The internal cells are called T cells (for Tree). All the L cells are identical; all the T cells are identical except for the root cell, which acts as an I/O port for the machine. (Since this would be too tight a bottleneck in a large machine, Mago suggests the possibility of allowing more I/O ports--all the T cells at some particular level of the tree, say.)

Other Reference Publication (1):
International Journal of Computer & Information Sciences 8, 5 (Oct. 1979) and 8, 6 (Dec. 1979) "A Network of Microprocessors to Execute Reduction Languages" Mago.

Other Reference Publication (2):
Communications of the ACM 21, 8 (Aug. 1978) pp. 613-641 Backus "Can Programming be Liberated from the Von Neuman Style".

☐ 105. Document ID: US 4538239 A

L2: Entry 105 of 108 File: USPT Aug 27, 1985

DOCUMENT-IDENTIFIER: US 4538239 A
TITLE: High-speed multiplier for microcomputer used in digital signal processing system

Brief Summary Text (3):
A microprocessor device is a central processing unit or CPU for a digital processor which is usually contained in a single semiconductor integrated circuit or "chip" fabricated by "MOS/LSI" technology, as shown in U.S. Pat. No. 3,757,306 issued to Gary W. Boone and assigned to Texas Instruments. The Boone patent shows a single-chip 8-bit CPU including a parallel ALU, registers for data and addresses, an instruction register and a control decoder, all interconnected using the Von Neuman architecture and employing a bidirectional parallel bus for data, address and instructions. U.S. Pat. No. 4,074,351, issued to Gary W. Boone and Michael J. Cochran, assigned to Texas Instruments, shows a single-chip "microcomputer" type device which contains a 4-bit parallel ALU and its control circuitry, with on-chip ROM for program storage and on-chip RAM for data storage, constructed in the Harvard architecture. The term microprocessor usually refers to a device employing external memory for program and data storage, while the term microcomputer refers to a device with on-chip ROM and RAM for program and data storage; the terms are also used interchangably, however, and are not intended as restrictive as to this invention.

Brief Summary Text (4):
Subsequent to 1971 when U.S. Pat. Nos. 3,757,306 and 4,074,351 were originally filed, many improvements have been made in microprocessors and microcomputers to increase the speed and capability of these devices and reduce the cost of manufacture, providing more circuitry and functions in less space, i.e., smaller chip size. Improved VLSI semiconductor processing and photolithographic techniques allow narrower line widths and higher resolution, providing added circuit density and higher speed, but circuit and system improvements also contribute to the goals of increased performance with smaller chip size. Some of these improvements in microcomputers are disclosed in the following U.S. Patents, all assigned to Texas Instruments: U.S. Pat. Nos. 3,991,305 issued to Edward R. Caudel and Joseph H. Raymond Jr.; 4,156,927 issued to David J. McElroy and Graham S. Tubbs; 3.934,233 issued to R. J. Fisher and G. D. Rogers; 3,921,142 issued to J. D. Bryant and G. A. Hartsell; 3,900,722 issued to M. J. Cochran and C. P. Grant; 3,932,846 issued to C. W. Brixey et al; 3,939,335 issued to G. L. Brantingham, L. H. Phillips and L. T. Novak; 4,125,901 issued to S. P. Hamilton, L. L. Miles, et al; 4,158,432 issued to M. G. VanBavel; 3,757,308 and 3,984,816. The devices described in these patents have been of the Harvard architecture and of the 4-bit type, particularly adapted for calculator or controller applications.

Brief Summary Text (5):
Additional examples of microprocessor and microcomputer devices in the evolutation of this technology are described in publications. In Electronics, Sept. 25, 1972, pp. 31-32, a 4-bit P-channel MOS microcomputer with on-chip ROM and RAM is shown which is similar to U.S. Pat. No. 3,991,305. Two of the most widely used 8-bit microprocessors like that of U.S. Pat. No. 3,757,306 are described in Electronics, Apr. 18, 1974 at pp. 88-95 (the Motorola 6800) and pp. 95-100 (the Intel 8080). A microcomputer version of the 6800 is described in Electronics, Feb. 2, 1978 at pp. 95-103. Likewise, a single-chip microcomputer version of the 8080 is shown in Electronics, Nov. 25, 1976 at pp. 99-105. Another single-chip microcomputer, the Mostek 3872, is shown in Electronics, May 11, 1978, at p. 105-110 and an improved version of the 6800 is disclosed in ELectronics, Sept. 17, 1979 at pp. 122-125. Sixteen-bit microprocessors based on minicomputer instruction sets evolved such as the part number TMS9900 described in a book entitled "9900 Family Systems Design", published in 1978 by Texas Instruments Incorporated, P.O. Box 1443, M/S 6404, Houston, Tex. 77001, Library of Congress Catalog No. 78-058005. The 8086, a 16-bit microprocessor evolving from the 8080, is described in Electronics, Feb. 16, 1978, pp. 99-104, while a 16-bit microprocessor identified as the 68000 (based on the 6800) is described in Electronic Design, Sept. 1, 1978 at pp. 100-107, and in IEEE Computer, Vol. 12, No. 2, pp. 43-52 (1979).

Brief Summary Text (6):
These prior 8-bit and 16-bit microprocessors and microcomputers have been general-purpose processors of the Von Neuman architecture with multiplexed address/data busses, and usually have been microcoded as described in U.S. patent application Ser. No. 209,915, filed Nov. 24, 1980 by Guttag, McDonough and Laws (now U.S. Pat. No. 4,402,043), or Ser. No. 253,624, filed Apr. 13, 1981, by Hayn, McDonough and Bellay, both assigned to Texas Instruments, and at pp. 28-34, IEEE Spectrum, March 1979, by McKevitt and Bayliss, or Proceedings 11th Annual Microprogramming Workshop, December, 1979 By Stintter and Tredenick. Microcoding, originally described by Wilkes in 1951, employs a control ROM to store microinstruction sequences entered by instruction words; the programmer works in a higher level machine code, so the number of assembly language code statements is supposedly reduced, and thus programming cost is reduced.

Brief Summary Text (7):
In contrast, a special-purpose high-speed microcomputer device according to the embodiment of the invention described herein departs from these contemporary microprocessor devices in several major respects in order to achieve substantial speed and performance advantages. This device is a non-microcoded processor of modified Harvard architecture.

Detailed Description Text (2):
MICROPROCESSOR SYSTEM

Detailed Description Text (5):
It is understood that, even though described in the context of a microcomputer in the preferred embodiment, with an on-chip program ROM 14 and data RAM 15, nevertheless some concepts of the invention may be used in a single-chip microprocessor with all off-chip program memory and/or data memory instead of the on-chip memory illustrated. Indeed, modes of operation are provided which disable the on-chip memory. Also, a microcomputer is shown having two separate external program address and data busses instead of the multiplexed, bidirectional busses which are now common, but some features herein disclosed are applicable where busses are multiplexed. The advantage of separating the busses and separating program and data memory space is speed.

Detailed Description Text (93):
The multiplier M, shifter S, ALU, accumulator Acc and auxiliary registers AR0, AR1 on the chip 10 of FIG. 4 comprise a 32-bit wide "strip" which is an array of rows (parallel to control lines #C) and columns (parallel to metal bus lines such as D-Bus and P-Bus and ALU and register bits) containing all of the 16-bit and 32-bit registers, ALU bits, and the like circuitry associated with the D-Bus and related control lines #C. As set forth in U.S. Pat. No. 4,402,044, issued to McDonough and Guttag, assigned to Texas Instruments, an important feature is that the 32-bit ALU and its associated 32-bit Acc registers, the two 16-bit AR registers, the shifter S, and the bus interchange BIM as described above are laid out on the MOS/LSI chip 10 in a regular strip pattern as seen in FIG. 4. Other circuitry connected to the D-Bus and the ALU-b input and having controls #C shared by sixteen or thirty-two bits may also be in the strip, such as AR and BIM. The Acc and the ALU each contain thirty-two bits or stages which are laid out in a regular pattern like memory cells, the bits arrayed and aligned horizontally and vertically as seen in FIG. 4. D-Bus and P-Bus of FIG. 2 are each sixteen parallel metal strips on top of the cells of the ALU and registers, and all of the dozens of control lines #C are horizontal polysilicon lines typically used as the control gates for transistors in the ALU and its associated registers and like circuitry. This layout arrangement is advantageous because the multiplier ALU and registers, and perpendicular control lines #C and metal busses fit in an array with virtually none of the wasted space used merely for routing conductors in conventional construction of microprocessors. Metal bus lines such as P-Bus and D-Bus and control lines #C are in large part routed over functional regions or cells of the chip in the strip rather than over unused silicon, and many 90 degree turns are produced inherently at functional cells rather than in conductor routing. In the prior devices, the controls, the registers, the ALU, etc. where islands of circuitry connected by busses or conductors. The enlarged view of FIG. 4a shows a small part of the strip, two-bits wide, illustrating the metal bus lines and the polysilicon control lines #C for an N-channel silicon gate MOS device made generally by a single-level polysilicon process according to U.S. Pat. No. 4,055,444, assigned to Texas Instruments. Various contacts (not shown) would be made within each register bit or stage from metal to silicon or to polysilicon. It is significant to note that many of the connecting lines from registers to busses illustrated in FIG. 2 are not physically lines or elongated conductors at all but instead are merely metal-to-silicon or metal-to-poly contact areas along the metal bus lines of FIG. 4a. That is, routing of 16-bit or 32-bit sets of parallel conductors is minimized by the strip feature, and the size of the chip 10 is reduced. All busses are not needed in any one part of the strip, and thus the pitch or maximum width of cells of the strip is minimized since the the metal-to-metal spacing is a critical limiting factor in bit density.

CLAIMS:

1. A single-chip microprocessor device containing a multiplier circuit, and containing clock means to generate repetitive machine state intervals, said multiplier circuit operating to produce a product of first and second operands in a single one of said machine state intervals, said multiplier circuit comprising:

(a) a first input register for holding said first operand of N bits; and means for loading said first operand in a first machine state interval;

(b) a second input means for holding said second operand of M bits during a second machine state interval following said first interval;

(c) N/2 static adder levels, each of said static adder levels including a control section having a plurality of inputs connected for receiving said control from said outputs of one of said decoder means, each level except the lowest containing at least M parallel binary adder stages, each stage of each level receiving one of said M bits from said second input means, the lowest level containing at least M adder stages receiving no carry input but only said controls and M bits, means for connecting partial products and carry from one level to the next higher level, but no carry being coupled along adder stages within a level.

(d) at least M+N dynamic adder stages, means for providing ripple carry along said dynamic adder stages, each stage receiving said partial product outputs from respective ones of said static adder levels, the MSB dynamic adder stages receiving partial product bits from the highest level of said static adder levels in a later part of a third machine state interval following said second machine state interval, the two LSB dynamic adder stages receiving two partial product bits from the lowest level of said static adder levels in an early part of said third machine state, and each pair of dynamic adder stages between LSBs and MSBs receiving two partial product bits from LSB stages of corresponding intervening static adder levels.

2. A microprocessor device having a multiplier circuit according to claim 1 wherein said decoders are identical Booth's decoders producing controls including add, subtract, shift and do-nothing.

3. A microprocessor device having a multiplier circuit according to claim 1 wherein said first input register is a temporary register loaded in said first machine state interval, and the second input means is a data bus loaded in said second machine state interval at which time said controls exist at said outputs of said decoder means.

4. A microprocessor device having a multiplier circuit according to claim 1 wherein the second level of the static adder levels employs half-adder stages and all higher levels employ full adder stages.

5. A microprocessor device having a multiplier circuit according to claim 4 wherein the lowest level of said static adder levels receives no partial product inputs and consists of only said control section.

6. A microprocessor device having a multiplier circuit according to claim 1 wherein said first input register is loaded in said first machine state interval, and the second input is a data bus loaded in said second machine state interval at which time said controls exist at the decoder outputs.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments

KWIC | Draw Desc | Image

☐ 106. Document ID: US 4528625 A

L2: Entry 106 of 108 File: USPT Jul 9, 1985

DOCUMENT-IDENTIFIER: US 4528625 A
TITLE: Input/output instruction execution in microcomputer

Brief Summary Text (3):
A microprocessor device is a central processing unit or CPU for a digital processor which is usually contained in a single semiconductor integrated circuit or "chip" fabricated by "MOS/LSI" technology, as shown in U.S. Pat. No. 3,757,306 issued to Gary W. Boone and assigned to Texas Instruments. The Boone patent shows a single-chip 8-bit CPU including a parallel ALU, registers for data and addresses, an instruciton register and a control decoder, all interconnected using the Von Neuman

architecture and employing a bidirectional parallel bus for data, address and instructions. U.S. Pat. No. 4,074,351, issued to Gary W. Boone and Michael J Cochran, assigned to Texas Instruments, shows a single-chip "microcomputer" type device which contains a 4-bit parallel ALU and its control circuitry, with on-chip ROM for program storage and on-chip RAM for data storage, constructed in the Harvard architecture. The term microprocessor usually refers to a device employing external memory for program and data storage, while the term microcomputer refers to a device with on-chip ROM and RAM for program and data storage; the terms are also used interchangably, however, and are not intended as restrictive as to this invention.

Brief Summary Text (4):
Subsequent to 1971 when Pat. Nos. 3,757,306 and 4,074,351 were originally filed, many improvements have been made in microprocessors and microcomputers to increase the speed and capability of these devices and reduce the cost of manufacture, providing more circuitry and functions in less space, i.e., smaller chip size. Improved VLSI semiconductor processing and photolithographic techniques allow narrower line widths and higher resolution, providing added circuit density and higher speed, but circuit and system improvements also contribute to the goals of increased performance with smaller chip size. Some of these improvements in microcomputers are disclosed in the following U.S. Patents, all assigned to Texas Instruments: No. 3,991,305 issued to Edward R. Caudel and Joseph H. Raymond Jr.; No. 4,156,927 issued to David J. McElroy and Graham S. Tubbs; No. 3,934,233 issued to R. J. Fisher and G. D. Rogers; No. 3,921,142 issued to J. D. Bryant and G. A. Hartsell; No. 3,900,722 issued to M. J. Cochran and C. P. Grant; No. 3,932,846 issued to C. W. Brixey et al; No. 3,939,335 issued to G. L. Brantingham, L. H. Phillips and L. T. Novak; No. 4,125,901 issued to S. P. Hamilton, L. L. Miles, et al; No. 4,158,432 issued to M. G. VanBavel; No. 3,757,308 and No. 3,984,816. The devices described in these patents have been of the Harvard architecture and of the 4-bit type, particularly adapted for calculator or controller applications.

Brief Summary Text (5):
Additional examples of microprocessor and microcomputer devices in the evolutation of this technology are described in publications. In Electronics, Sept. 25, 1972, pp. 31-32 a 4-bit P-channel MOS microcomputer with on-chip ROM and RAM is shown which is similar to Pat. No. 3,991,305. Two of the most widely used 8-bit microprocessors like that of Pat. No. 3,757,306 are described in Electronics, Apr. 18, 1974 at pp. 88-95 (the Motorola 6800) and pp. 95-100 (the Intel 8080). A microcomputer version of the 6800 is described in Electronics, Feb. 2, 1978 at pp. 95-103. Likewise, a single-chip microcomputer version of the 8080 is shown in Electronics, Nov. 25, 1976 at pp. 99-105. Another single-chip microcomputer, the Mostek 3872, is shown in Electronics, May 11, 1978, at p. 105-110 and an improved version of the 6800 is disclosed in Electronics, Sept. 17, 1979 at pp. 122-125. Sixteen-bit microprocessors based on minicomputer instruction sets evolved such as the part number TMS9900 described in a book entitled "9900 Family Systems Design", published in 1978 by Texas Instruments Incorporated, P.O. Box 1443, M/S 6404, Houston, Tex. 77001, Library of Congress Catalog No. 78-058005. The 8086, a 16-bit microprocessor evolving from the 8080, is described in Electronics, Feb. 16, 1978, pp. 99-104, while a 16-bit microprocessor identified as the 68000 (based on the 6800) is described in Electronic Design, Sept. 1, 1978 at pp. 100-107, and in IEEE Computer, Vol. 12. No. 2, pp. 43-52 (1979).

Brief Summary Text (6):
These prior 8-bit and 16-bit microprocessors and microcomputers have been general-purpose processors of the Von Neuman architecture with multiplexed address/data busses, and usually have been microcoded as described in U.S. patent application Ser. No. 209,915, filed Nov. 24, 1980 by Guttag, McDonough and Laws, (now U.S. Pat. 4,402,043), or Ser. No. 253,624, filed Apr. 13, 1981, by Hayn, McDonough and Bellay, both assigned to Texas Instruments, and at pp. 28-34, IEEE Spectrum, March 1979, by McKevitt and Bayliss, or Proceedings 11th Annual Microprogramming Workshop, December, 1979 by Stintter and Tredenick. Microcoding, originally described by Wilkes in 1951, employs a control ROM to store microinstruction sequences entered by instruction words; the programmer works in a higher level machine code, so the number of assembly language code statements is supposedly reduced, and thus programming cost is reduced.

Brief Summary Text (7):
In contrast, a special-purpose high-speed microcomputer device according to the embodiment of the invention described herein departs from these contemporary microprocessor devices in several major respects in order to achieve substantial speed and performance advantages. This device is a non-microcoded processor of modified Harvard architecture.

Detailed Description Text (2):
MICROPROCESSOR SYSTEM

Detailed Description Text (5):
It is understood that, even though described in the context of a microcomputer in the preferred embodiment, with an on-chip program ROM 14 and data RAM 15, nevertheless some concepts of the invention may be used in a single-chip microprocessor with all off-chip program memory and/or data memory instead of the on-chip memory illustrated. Indeed, modes of operation are provided which disable the on-chip memory. Also, a microcomputer is shown having two separate external program address and data busses instead of the multiplexed, bidirectional busses which are now common, but some features herein disclosed are applicable where busses are multiplexed. The advantage of separating the busses and separating program and data memory space is speed.

Detailed Description Text (93):
The multiplier M, shifter S, ALU, accumulator Acc and auxiliary registers AR0, AR1 on the chip 10 of FIG. 4 comprise a 32-bit wide "strip" which is an array of rows (parallel to control lines #C) and columns (parallel to metal bus lines such as D-Bus and P-Bus and ALU and register bits) containing all of the 16-bit and 32-bit registers, ALU bits, and the like circuitry associated with the D-Bus and related control lines #C. As set forth in U.S. Pat. No. 4,402,044, issued to McDonough and Guttag, assigned to Texas Instruments, an important feature is that the 32-bit ALU and its associated 32-bit Acc registers, the two 16-bit AR registers, the shifter S, and the bus interchange BIM as described above are laid out on the MOS/LSI chip 10 in a regular strip pattern as seen in FIG. 4. Other circuitry connected to the D-Bus and the ALU-b input and having controls #C shared by sixteen or thirty-two bits may also be in the strip, such as AR and BIM. The Acc and the ALU each contain thirty-two bits or stages which are laid out in a regular pattern like memory cells, the bits arrayed and aligned horizontally and vertically as seen in FIG. 4. D-Bus and P-Bus of FIG. 2 are each sixteen parallel metal strips on top of the cells of the ALU and registers, and all of the dozens of control lines #C are horizontal polysilicon lines typically used as the control gates for transistors in the ALU and its associated registers and like circuitry. This layout arrangement is advantageous because the multiplier ALU and registers, and perpendicular control lines #C and metal busses fit in an array with virtually none of the wasted space used merely for routing conductors in conventional construction of microprocessors. Metal bus lines such as P-Bus and D-Bus and control lines #C are in large part routed over functional regions or cells of the chip in the strip rather than over unused silicon, and many 90 degree turns are produced inherently at functional cells rather than in conductor routing. In the prior devices, the controls, the registers, the ALU, etc. where islands of circuitry connected by busses or conductors. The enlarged view of FIG. 4a shows a small part of the strip, two-bits wide, illustrating the metal bus lines and the polysilicon control lines #C for an N-channel silicon gate MOS device made generally by a single-level polysilicon process according to U.S. Pat. No. 4,055,444, assigned to Texas Instruments. Various contacts (not shown) would be made within each register bit or stage from metal to silicon or to polysilicon. It is significant to note that many of the connecting lines from registers to busses illustrated in FIG. 2 are not physically lines or elongated conductors at all but instead are merely metal-to-silicon or metal-to-poly contact areas along the metal bus lines of FIG. 4a. That is, routing of 16-bit or 32-bit sets of parallel conductors is minimized by the strip feature, and the size of the chip 10 is reduced. All busses are not needed in any one part of the strip, and thus the pitch or maximum width of cells of the strip is minimized since the the metal-to-metal spacing is a critical limiting factor in bit density.

☐ 107. Document ID: US 4507727 A

L2: Entry 107 of 108 File: USPT Mar 26, 1985

DOCUMENT-IDENTIFIER: US 4507727 A
TITLE: Microcomputer with ROM test mode of operation

Brief Summary Text (3):
A microprocessor device is a central processing unit or CPU for a digital processor which is usually contained in a single semiconductor integrated circuit or "chip" fabricated by "MOS/LSI" technology, as shown in U.S. Pat. No. 3,757,306 issued to Gary W. Boone and assigned to Texas Instruments. The Boone patent shows a single-chip 8-bit CPU including a parallel ALU, registers for data and addresses, an instruction register and a control decoder, all interconnected using the Von Neuman architecture and employing a bidirectional parallel bus for data, address and instructions. U.S. Pat. No. 4,074,351, issued to Gary W. Boone and Michael J. Cochran, assigned to Texas Instruments, shows a single-chip "microcomputer" type device which contains a 4-bit parallel ALU and its control circuitry, with on-chip ROM for program storage and on-chip RAM for data storage, constructed in the Harvard architecture. The term microprocessor usually refers to a device employing external memory for program and data storage, while the term microcomputer refers to a device with on-chip ROM and RAM for program and data storage; the terms are also used interchangable, however, and are not intended as restrictive as to this invention.

Brief Summary Text (4):
Subsequent to 1971 when U.S. Pat. Nos. 3,757,306 and 4,074,351 were originally filed, many improvements have been made in microprocessors and microcomputers to increase the speed and capability of these devices and reduce the cost of manufacture, providing more circuitry and functions in less space, i.e., smaller chip size. Improved VLSI semiconductor processing and photolithographic techniques allow narrower line widths and higher resolution, providing added circuit density and higher speed, but circuit and system improvements also contribute to the goals of increased performance with smaller chip size. Some of these improvements in microcomputers are disclosed in the following U.S. patents, all assigned to Texas Instruments: U.S. Pat. Nos. 3,991,305 issued to Edward R. Caudel and Joseph H. Raymond Jr.; 4,156,927 issued to David J. McElroy and Graham S. Tubbs; 3,934,233 issued to R. J. Fisher and G. D. Rogers; 3,921,142 issued to J. D. Bryant and G. A. Hartsell; 3,900,722 issued to M. J. Cochran and C. P. Grant; 3,932,846 issued to C. W. Brixey et al; 3,939,335 issued to G. L. Brantingham, L. H. Phillips and L. T. Novak; 4,125,901 issued to S. P. Hamilton, L. L. Miles, et al; 4,158,432 issued to M. G. VanBavel; 3,757,308 and 3,984,816. The devices described in these patents have been of the Harvard architecture and of the 4-bit type, particularly adapted for calculator or controller applications.

Brief Summary Text (5):
Additional examples of microprocessor and microcomputer devices in the evolutation of this technology are described in publications. In Electronics, Sept. 25, 1972, pp. 31-32, a 4-bit P-channel MOS microcomputer with on-chip ROM and RAM is shown which is similar to U.S. Pat. No. 3,991,305. Two of the most widely used 8-bit microprocessors like that of U.S. Pat. No. 3,757,306 are described in Electronics, Apr. 18, 1974 at pp. 88-95 (the Motorola 6800) and pp. 95-100 (the Intel 8080). A microcomputer version of the 6800 is described in Electronics, Feb. 2, 1978 at pp. 95-103. Likewise, a single-chip microcomputer version of the 8080 is shown in Electronics, Nov. 25, 1976 at pp. 99-105. Another single-chip microcomputer, the Mostek 3872, is shown in Electronics, May 11, 1978, at p. 105-110 and an improved version of the 6800 is disclosed in Electronics, Sept. 17, 1979 at pp. 122-125. Sixteen-bit microprocessors based on minicomputer instruction sets evolved such as the part number TMS9900 described in a book entitled "9900 Family Systems Design", published in 1978 by Texas Instruments Incorporated, P.O. Box 1443, M/S 6404, Houston, Tex. 77001, Library of Congress Catalog No. 78-058005. The 8086, a 16-bit

microprocessor evolving from the 8080, is described in Electronics, Feb. 16, 1978, pp. 99-104, while a 16-bit microprocessor identified as the 68000 (based on the 6800) is described in Electronic Design, Sept. 1, 1978 at pp. 100-107, and in IEEE Computer, Vol. 12. No. 2, pp. 43-52 (1979).

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These prior 8-bit and 16-bit microprocessors and microcomputers have been general-purpose processors of the Von Neuman architecture with multiplexed address/data busses, and usually have been microcoded as described in U.S. patent applications Ser. No. 209,915, filed Nov. 24, 1980 by Guttag, McDonough and Laws (now U.S. Pat. No. 4,402,043), or Ser. No. 253,624, filed Apr. 13, 1981, by Hayn, McDonough and Bellay, both assigned to Texas Instruments, and at pp. 28-34, IEEE Spectrum, March 1979, by McKevitt and Bayliss, or Proceedings 11th Annual Microprogramming Workshop, December, 1979 by Stintter and Tredenick. Microcoding, originally described by Wilkes in 1951, employs a control ROM to store microinstruction sequences entered by instruction words; the programmer works in a higher level machine code, so the number of assembly language code statements is supposedly reduced, and thus programming cost is reduced.

Brief Summary Text (7):
In contrast, a special-purpose high-speed microcomputer device according to the embodiment of the invention described herein departs from these contemporary microprocessor devices in several major respects in order to achieve substantial speed and performance advantages. This device is a non-microcoded processor of modified Harvard architecture.

Detailed Description Text (2):
MICROPROCESSOR SYSTEM

Detailed Description Text (5):
It is understood that, even though described in the context of a microcomputer in the preferred embodiment, with an on-chip program ROM 14 and data RAM 15, nevertheless some concepts of the invention may be used in a single-chip microprocessor with all off-chip program memory and/or data memory instead of the on-chip memory illustrated. Indeed, modes of operation are provided which disable the on-chip memory. Also, a microcomputer is shown having two separate external program address and data busses instead of the multiplexed, bidirectional busses which are now common, but some features herein disclosed are applicable where busses are multiplexed. The advantage of separating the busses and separating program and data memory space is speed.

Detailed Description Text (93):
The multiplier M, shifter S, ALU, accumulator Acc and auxiliary registers AR0, AR1 on the chip 10 of FIG. 4 comprise a 32-bit wide "strip" which is an array of rows (parallel to control lines #C) and columns (parallel to metal bus lines such as D-Bus and P-Bus and ALU and register bits) containing all of the 16-bit and 32-bit registers, ALU bits, and the like circuitry associated with the D-Bus and related control lines #C. As set forth in U.S. Pat. No. 4,402,044, issued to McDonough and Guttag, assigned to Texas Instruments, an important feature is that the 32-bit ALU and its associated 32-bit Acc registers, the two 16-bit AR registers, the shifter S, and the bus interchange BIM as described above are laid out on the MOS/LSI chip 10 in a regular strip pattern as seen in FIG. 4. Other circuitry connected to the D-Bus and the ALU-b input and having controls #C shared by sixteen or thirty-two bits may also be in the strip, such as AR and BIM. The Acc and the ALU each contain thirty-two bits or stages which are laid out in a regular pattern like memory cells, the bits arrayed and aligned horizontally and vertically as seen in FIG. 4. D-Bus and P-Bus of FIG. 2 are each sixteen parallel metal strips on top of the cells of the ALU and registers, and all of the dozens of control lines #C are horizontal polysilicon lines typically used as the control gates for transistors in the ALU and its associated registers and like circuitry. This layout arrangement is advantageous because the multiplier ALU and registers, and perpendicular control lines #C and metal busses fit in an array with virtually none of the wasted space used merely for routing conductors in conventional contruction of microprocessors. Metal bus lines such as P-Bus and D-Bus and control lines #C are in large part routed over functional regions or cells of the chip in the strip rather than over unused

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Other Reference Publication (1):
Cukier, M. et al., "Test Device for Microprocessor Programming" IBM Tech. Discl. Bulletin, vol. 21, No. 10, Mar. 1979.

☐ 108. Document ID: US 4503500 A

L2: Entry 108 of 108 File: USPT Mar 5, 1985

DOCUMENT-IDENTIFIER: US 4503500 A
TITLE: Microcomputer with bus interchange module

Brief Summary Text (3):
A microprocessor device is a central processing unit or CPU for a digital processor which is usually contained in a single semiconductor integrated circuit or "chip" fabricated by "MOS/LSI" technology, as shown in U.S. Pat. No. 3,757,306 issued to Gary W. Boone and assigned to Texas Instruments. The Boone patent shows a single-chip 8-bit CPU including a parallel ALU, registers for data and addresses, an instruction register and a control decoder, all interconnected using the Von Neuman architecture and employing a bidirectional parallel bus for data, address and instructions. U.S. Pat. No. 4,074,351, issued to Gary W. Boone and Michael J. Cochran, assigned to Texas Instruments, shows a single-chip "microcomputer" type device which contains a 4-bit parallel ALU and its control circuitry, with on-chip ROM for program storage and on-chip RAM for data storage, constructed in the Harvard architecture. The term microprocessor usually refers to a device employing external memory for program and data storage, while the term microcomputer refers to a device with on-chip ROM and RAM for program and data storage; the terms are also used interchangably, however, and are not intended as restrictive as to this invention.

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Subsequent to 1971 when U.S. Pat. Nos. 3,757,306 and 4,074,351 were originally filed, many improvements have been made in microprocessors and microcomputers to increase the speed and capability of these devices and reduce the cost of manufacture, providing more circuitry and functions in less space, i.e., smaller chip size. Improved VLSI semiconductor processing and photolithographic techniques allow narrower line widths and higher resolution, providing added circuit density and higher speed, but circuit and system improvements also contribute to the goals of increased performance with smaller chip size. Some of these improvements in microcomputers are disclosed in the following U.S. Patents, all assigned to Texas Instruments: U.S. Pat. No. 3,991,305 issued to Edward R. Caudel and Joseph H. Raymond Jr.; U.S. Pat. No. 4,156,927 issued to David J. McElroy and Graham S. Tubbs;

U.S. Pat. No. 3,934,233 issued to R. J. Fisher and G. D. Rogers; U.S. Pat. No. 3,921,142 issued to J. D. Bryant and G. A. Hartsell; U.S. Pat. No. 3,900,722 issued to M. J. Cochran and C. P. Grant; U.S. Pat. No. 3,932,846 issued to C. W. Brixely et al; U.S. Pat. No. 3,939,335 issued to G. L. Brantingham, L. H. Phillips and L. T. Novak; U.S. Pat. No. 4,125,901 issued to S. P. Hamilton, L. L. Miles, et al; U.S. Pat. No. 4,158,432 issued to M. G. VanBavel; U.S. Pat. No. 3,757,308 and U.S. Pat. No. 3,984,816. The devices described in these patents have been of the Harvard architecture and of the 4-bit type, particularly adapted for calculator or controller applications.

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Detailed Description Text (2):
Microprocessor System

Detailed Description Text (5):
It is understood that, even though described in the context of a microcomputer in the preferred embodiment, with an on-chip program ROM 14 and data RAM 15, nevertheless, some concepts of the invention may be used in a single-chip microprocessor with all off-chip program memory and/or data memory instead of the on-chip memory illustrated. Indeed, modes of operation are provided which disable the on-chip memory. Also, a microcomputer is shown having two separate external program address and data busses instead of the multiplexed, bidirectional busses which are now common, but some features herein disclosed are applicable where busses are multiplexed. The advantage of separating the busses and separating program and

data memory space is speed.

Detailed Description Text (92):
The multiplier M, shifter S, ALU, accumulator Acc and auxiliary registers AR0, AR1 on the chip 10 of FIG. 4 comprise a 32-bit wide "strip" which is an array of rows (parallel to control lines #C) and columns (parallel to metal bus lines such as D-Bus and P-Bus and ALU and register bits) containing all of the 16-bit and 32-bit registers, ALU bits, and the like circuitry associated with the D-Bus and related control lines #C. As set forth in U.S. Pat. No. 4,402,044 issued to McDonough and Guttag, assigned to Texas Instruments, an important feature is that the 32-bit ALU and its associated 32-bit Acc registers, the two 16-bit AR registers, the shifter S, and the bus interchange BIM as described above are laid out on the MOS/LSI chip 10 in a regular strip pattern as seen in FIG. 4. Other circuitry connected to the D-Bus and the ALU-b input and having controls #C shared by sixteen or thirty-two bits may also be in the strip, such as AR and BIM. The Acc and the ALU each contain thirty-two bits or stages which are laid out in a regular pattern like memory cells, the bits arrayed and aligned horizontally and vertically as seen in FIG. 4. D-Bus and P-Bus of FIG. 2 are each sixteen parallel metal strips on top of the cells of the ALU and registers, and all of the dozens of control lines #C are horizontal polysilicon lines typically used as the control gates for transistors in the ALU and its associated registers and like circuitry. This layout arrangement is advantageous because the multiplier ALU and registers, and perpendicular control lines #C and metal busses fit in an array with virtually none of the wasted space used merely for routing conductors in conventional contruction of microprocessors. Metal bus lines such as P-Bus and D-Bus and control lines #C are in large part routed over functional regions or cells of the chip in the strip rather than over unused silicon, and many 90 degree turns are produced inherently at functional cells rather than in conductor routing. In the prior devices, the controls, the registers, the ALU, etc. where islands of circuitry connected by busses or conductors. The enlarged view of FIG. 4a shows a small part of the strip, two-bits wide, illustrating the metal bus lines and the polysilicon control lines #C for an N-channel silicon gate MOS device made generally by a single-level polysilicon process according to U.S. Pat. No. 4,055,444, assigned to Texas Instruments. Various contacts (not shown) would be made within each register bit or stage from metal to silicon or to polysilicon. It is significant to note that many of the connecting lines from registers to busses illustrated in FIG. 2 are not physically lines or elongated conductors at all but instead are merely metal-to-silicon or metal-to-poly contact areas along the metal bus lines of FIG. 4a. That is, routing of 16-bit or 32-bit sets of parallel conductors is minimized by the strip feature, and the size of the chip 10 is reduced. All busses are not needed in any one part of the strip, and thus the pitch or maximum width of cells of the strip is minimized since the the metal-to-metal spacing is a critical limiting factor in bit density.

Term	Documents
VON.USPT.	42055
VONS.USPT.	59
NEUMAN.USPT.	3426
NEUMEN.USPT.	5
NEUMENS	0
NEUMANS.USPT.	1
MICROPROCESSOR$	0
MICROPROCESSOR.USPT.	133457
MICROPROCESSORAND.USPT.	1
MICROPROCESSORBASED.USPT.	29
MICROPROCESSORCONTROLLED.USPT.	7
(MICROPROCESSOR$ AND (VON ADJ NEUMAN)).USPT.	108

There are more results than shown above. Click here to view the entire set.

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